Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **RFIN**
2. **VDD**
3. **RFOUT**

**.120”**

**H9301 HMC**

**2**

**1**

**3**

**.051”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004 x .004”**

**Backside Potential: GND**

**Mask Ref: H9301**

**APPROVED BY: DK DIE SIZE .051” X .120” DATE: 3/8/23**

**MFG: HITTITE THICKNESS .004” P/N: HMC462**

**DG 10.1.2**

#### Rev B, 7/1